CLAIMS

What is claimed is:

1. A network communications system, comprising:

a switch having a first plurality of ports;

a second plurality of line cards, each line card coupled to at least one of the ports;

wherein each line card includes a test generator; each test generator comprising a test pattern generator operable to produce and transmit at least two traffic flows, and further comprising a receiver operable to produce at least two expected traffic flows, to receive at least two transmitted traffic flows and to compare the received traffic flows to the expected traffic flows.

2. The network communications system of Claim 1, wherein each test pattern generator further comprises a plurality of registers which define the size and contents of the at least two traffic flows.

3. The network communications system of Claim 2, wherein each test pattern generator further comprises a state machine for controlling the construction and transmission of the at least two traffic flows, and for controlling the insertion of unique packet headers into each of the at least two traffic flows.

4. The network communications system of Claim 1, wherein the received traffic flows originate at a first one of the first plurality of ports, and are received from a second one of the first plurality of ports.

5. The network communications system of Claim 4, wherein the test generator is integrated on a single chip, the single chip being disposed on the line card.

6. A method of full speed in-circuit testing of a multi-port network communication switch, comprising:

coupling, to each port of the multi-port communication switch, one of a first plurality of line cards, each line card comprising a test generator, and each test generator comprising a test packet transmitter and a test packet receiver;

operating a first test generator coupled to a first port of the multi-port communication switch, to generate at least two traffic flows destined for a second port of the multi-port communication switch, and to transmit those at least two traffic flows; and

operating a second test generator coupled to the second port to generate a local copy of at least two expected traffic flows, to receive the at least two traffic flows, and to compare the at least two expected traffic flows with the at least two received traffic flows.

7. The method of Claim 6, further comprising recording an error if any one of the at least two received traffic flows do not match the expected flows.

8. The method of Claim 6, further comprising transmitting a synchronization packet from the first test generator coupled to the first port to the second test generator coupled to the second port.

9. The method of Claim 6, wherein the first port and the second port are different ports of the switch.

10. The method of Claim 7, wherein each of the at least two traffic flows includes a packet header and each of the packet headers are different.

11. The method of Claim 6, wherein operating the second test generator further comprises setting a flag indicative of an out-of-synchronization state; receiving at least one packet; comparing the at least one packet to an expected pattern, and setting a flag indicative of a synchronized state if the comparison of the received and expected data results in a match.

12. The method of Claim 11, wherein an end of packet flag is received at the end of a packet.

13. The method of Claim 11, wherein the at least one packet comprises a first predetermined integer number of packets.

14. The method of Claim 13, further comprising setting the flag indicative of an out-of-synchronization state if a second predetermined integer number of packets fail to match the expected data.

15. The method of Claim 7, further comprising programming at least one packet header for the test packet transmitter, and programming at least one packet header for the test packet receiver.

16. A method for testing network communication equipment with a test packet generator, comprising:

a) transmitting, from the test packet generator, a synchronization packet;

b) generating a first data packet including a first header and a first payload;

c) transmitting, from the test packet generator, the first data packet;

d) providing a first inter-packet gap of a first length;

e) generating a second data packet including a second header and a second payload;

f) transmitting, from the test packet generator, the second data packet;

g) providing a second inter-packet gap of a second length; and

g) repeating steps (b) through (g) at least once;

wherein the first header is different from the second header.

17. The method of Claim 16, wherein the first length and the second length are different.

18. The method of Claim 17, wherein the first payload and the second payload are different.

19. The method of Claim 18, further comprising counting the number of packets transmitted by the test packet generator.

20. The method of Claim 16, wherein transmitting from the test packet generator comprises communicating data onto a parallel bus.

21. The method of Claim 16, further comprising counting the number of packets transmitted, receiving the packets, counting the received packets, and counting the received packets with errors; wherein the first and second inter-packet gaps are each an integer multiple of 8 bytes, the first header and second header are each 20 bytes longs, and the first and second headers contain different data, and wherein the size of the first packet is representative of a control packet on an Internet backbone,

and the size of the second packet is representative of a data packet on the Internet backbone.

22. The method of Claim 21, further comprising programming the content of the first packet header and the second packet header by executing software which results in writing to at least two sets of packet header registers.

23. The method of Claim 22, further comprising programming the content of the first payload and the second payload by executing software which results in setting one or more bits in at least two payload pattern registers.

24. The method of Claim 23, further comprising programming the size of the first packet and the second packet by executing software which results in writing packet size control information into at least two packet size control registers.

25. A method of testing network communications equipment, comprising:

a) programming a first set of registers that define a format of a first test packet;

b) programming a second set of registers that define a format of second test packet;

c) transmitting a synchronization packet;

d) transmitting the first test packet; and

e) transmitting, after a first inter-packet gap, the second test packet;

wherein the first test packet comprises a first packet header, and a first payload; and the second test packet comprises a second packet header, and a second payload.

26. The method of Claim 25, wherein the first and second packet headers are different.

27. The method of Claim 26, further comprising, after a second inter-packet gap, transmitting the first test packet.

28. The method of Claim 27, further comprising after a second occurrence of the first inter-packet gap, transmitting the second packet.

29. The method of Claim 28, wherein the first payload and the second payload are different.

30. The method of Claim 28, wherein the first payload and the second payload are the same.

31. The method of Claim 27, wherein programming the first set of registers comprises writing data into one or more registers so as to define:

1) a total number of bytes in the first test packet;

2) a size of a gap between the transmission of the first and second test packets;

3) a pattern used to fill the first payload; and

4) a content of the first header.

32. The method of Claim 27, wherein programming the second set of registers comprises writing data into one or more registers so as to define:

1) a total number of bytes in the second test packet;

2) a size of a gap between the transmission of the second and first test packets;

3) a pattern used to fill the second payload; and

4) a content of the second header.

33. The method of Claim 26, further comprising receiving the synchronization packet, receiving the first test packet, receiving the second test packet, incrementing a first counter to record the number of received packets; determining if the first test packet was received correctly, and determining if the second test packet was received correctly.

34. The method of Claim 33, further comprising incrementing a second counter if any received test packet contains an error.

35. The method of Claim 33, further comprising incrementing a third counter each for each test packet that is transmitted by the test generator.

36. The method of Claim 33, wherein transmitting the synchronization packet and receiving the synchronization packet are performed on a single chip.

37. The method of Claim A33, wherein transmitting the synchronization packet is performed on a first integrated circuit chip, and receiving the synchronization packet is performed on a second chip.

38. A test pattern generator suitable for integration in an integrated circuit, comprising:

a controller, the controller comprising a first and a second packet configuration register; a first and a second packet size register; a first and a second gap size register; a first and a second pattern register; a first and a second set of

packet header registers; a first and a second status/counter control register; a first and a second transmit packet counter; a first and a second receive packet counter; and a first and a second error counter.

39. The test pattern generator of Claim 38, further comprising a transmitter coupled to the controller and further coupled to a first data bus; and a receiver coupled to the controller and further coupled to a second data bus.

40. The test pattern generator of Claim 39, further comprising, a microcontroller interface adapted to communicatively couple the registers and counters to a stored program machine.

41. The test pattern generator of Claim 40, wherein the stored program machine is a microcontroller.

42. The test pattern generator of Claim 39, wherein the controller further comprises a first state machine adapted to produce one or more transmitter control signals.

43. The test pattern generator of Claim 42, wherein the controller further comprises a second state machine adapted to produce one or more receiver control signals.

44. The test pattern generator of Claim 43, wherein the controller, transmitter and receiver are all present on a single chip.

45. The test pattern generator of Claim 44, further comprising a quasi random static sequence generator.

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